OIPE JC50 APR 07 2005 PATENT & TRADEMARK OFFICE

04-11-05

IDW 4/4

PTO/SB/21 (04-04)

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/820,964
Filing Date	April 7, 2004
First Named Inventor	FUJIMOTO, Kazuhisa
Art Unit	2123
Examiner Name	Unassigned
Attorney Docket Number	16869P-112600US

Total Number of Pages in This Submission

ENCLOSURES *(Check all that apply)*

- ☒ Fee Transmittal Form (in duplicate)
- ☐ Fee Attached
- ☐ Preliminary Amendment
- ☐ After Final
- ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
- ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☒ Petition to Make Special (10 pages)
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
- ☐ After Allowance Communication to Technology Center (TC)
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) (please identify below):

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Eight (8) cited references

Remarks The Commissioner is authorized to charge any additional fees to Deposit Account 20-1430.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Townsend and Townsend and Crew LLP Chun-Pok Leung Reg. No. 41,405
Signature	
Date	April 7, 2005

CERTIFICATE OF TRANSMISSION/MAILING

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OIPE APR 07 2005 JC500 PATENT & TRADEMARK OFFICE

PTO/SB/17 (10-03)

FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 130.00

Complete if Known	
Application Number	10/820,964
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METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit Card ☐ Money Order ☐ Other ☐ None

☒ Deposit Account:

Deposit Account Number: 20-1430

Deposit Account Name: Townsend and Townsend and Crew LLP

The Director is authorized to: *(check all that apply)*

☒ Charge fee(s) indicated below ☒ Credit any overpayments

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($)0.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims		Fee from below	Fee Paid
Total Claims		-** =		X	=	
Independent Claims		-** =		X	=	
Multiple Dependent				X	=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)0.00

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive – unavoidable	
1453	1,330	2453	665	Petition to revive – unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	130
1807	50	1807	50	Petitions related to provisional applications	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR § 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) ----------

*Reduced by Basic Filing Fee Paid **SUBTOTAL (3)** ($)130.00

SUBMITTED BY				Complete *(if applicable)*	
Name (Print/Type)	Chun-Pok Leung	*Registration No. (Attorney/Agent)*	41,405	*Telephone*	650-326-2400
Signature				*Date*	April 7, 2005

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PATENT
Attorney Docket No.: 16869P-112600US
Client Ref. No.: 340400008US01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

KAZUHISA FUJIMOTO et al.

Application No.: 10/820,964

Filed: April 7, 2004

For: STORAGE SYSTEM

Customer No.: 20350

Examiner: Unassigned

Technology Center/Art Unit: 2123

Confirmation No.: 9555

PETITION TO MAKE SPECIAL FOR NEW APPLICATION UNDER M.P.E.P. § 708.02, VIII & 37 C.F.R. § 1.102(d)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is a petition to make special the above-identified application under MPEP § 708.02, VIII & 37 C.F.R. § 1.102(d). The application has not received any examination by an Examiner.

(a) The Commissioner is authorized to charge the petition fee of $130 under 37 C.F.R. § 1.17(i) and any other fees associated with this paper to Deposit Account 20-1430.

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~~01 FC:1464 130.00 DA~~

04/12/2005 AWONDAF1 00000102 201430 10820964
01 FC:1464 130.00 DA

(b) All the claims are believed to be directed to a single invention. If the Office determines that all the claims presented are not obviously directed to a single invention, then Applicants will make an election without traverse as a prerequisite to the grant of special status.

(c) Pre-examination searches were made of U.S. issued patents, including a classification search, a foreign patent database search, and a literature search. The searches were performed on or around February 26, 2005, and were conducted by a professional search firm, Mattingly, Stanger & Malur, P.C. The classification search covered Class 710 (subclasses 100, 300, and 305) and Class 711 (subclasses 100 and 114). Because of the large size of these subclasses, keywords were used to narrow of number of documents returned. The foreign patent database search was conducted using Espacenet in international subclass G06F1/26, directed to power supply means, e.g., regulating of, for data processing equipment. The literature search was performed using DIALOG online databases. The inventors further provided two references considered most closely related to the subject matter of the present application (see references #7-8).

(d) The following references, copies of which are attached herewith, are deemed most closely related to the subject matter encompassed by the claims:

(1) U.S. Patent No. 6,820,171 B1;

(2) U.S. Patent Publication No. 2002/0188786 A1;

(3) U.S. Patent Publication No. 2004/0098529 A1;

(4) U.S. Patent Publication No. 2004/0177182 A1;

(5) U.S. Patent Publication No. 2004/0199719 A1;

(6) U.S. Patent Publication No. 2005/0010715 A1;

(7) U.S. Patent No. 6,385,681; and

(8) U.S. Patent No. 6,542,961.

(e) Set forth below is a detailed discussion of references which points out with particularity how the claimed subject matter is distinguishable over the references.

A. Claimed Embodiments of the Present Invention

The claimed embodiments relate to a storage device having a configuration that is expandable from a small scale to a larger scale.

Independent claim 1 recites a storage device that includes an interface unit for connecting an external device, and a memory unit for storing data received at the interface unit. Also included are a processor unit that controls to store data received at the interface unit to the memory unit, and plural disk units in which the data stored in the memory unit is stored by the processor unit. The interface unit, the memory unit, and the processor unit are connected by a first backplane. The first backplane has plural first connectors for increasing or decreasing the number of the processing units, and the plural disk units are connected by a second backplane.

Independent claim 7 recites a storage device including an interface unit for connecting an external device, and a memory unit for storing data received at the interface unit. Also included are a processor unit that controls to store data received at the interface unit to the memory unit, and plural disk units in which the data stored in the memory unit is stored by the processor unit. The interface unit, the memory unit, and the processor unit are connected by a first backplane. The first backplane has plural first connectors for increasing or decreasing the interface units, and the plural disk units are connected by a second backplane.

Independent claim 13 recites a storage device that includes an interface unit connected to an external device, and that receives data from the external device. Also included are a memory unit that stores data received at the interface unit, plural disk units in which the data stored in the memory unit is stored by a processor unit, and a processor unit that stores data received at the interface unit to the memory unit, or controls to store data stored in the memory unit to the plural disk units. It is possible to increase or decrease the number of processor units in the case that the interface unit is not increased or decreased.

Independent claim 17 recites a storage device that includes an interface unit for connecting an external device, and a memory unit for storing data received at the interface unit. Also included are a processor unit that controls to store data received at the interface unit to the memory unit, and plural disk units in which the data stored in the memory unit is

stored by the processor unit. The interface unit, the memory unit, the processor unit, and the disk unit are each mounted on a first board, a second board, a third board, and a fourth board, respectively. The first board, the second board and the third board are connected by a first backplane, while the fourth board is connected by a second backplane.

In embodiments of the present invention, a storage device includes an interface unit for connecting an external device; a memory unit for storing data received at the interface unit; a processor unit that controls to store data received; and plural disk units to store the data. The interface unit, the memory unit, and the processor unit are connected by a first backplane. The first backplane has plural first connectors for increasing or decreasing the number of processor units or the number of interface units. The plural disk units are connected by a second backplane. The use of separate expandable backplanes enables the mounting of separate control unit chassis and disk unit chassis, and increases modularity of the system and makes possible separation of the disk unit from the control unit. This makes it possible to construct a storage system according to system scale, number of connected servers, number of connected hard drives, and the performance requirements. See, e.g., FIGS. 14 and 15, and discussion beginning at page 24 of the specification.

These advantages of the invention are realized in the claims 1 and 7 which set forth a storage device having a first backplane having plural connectors for increasing or decreasing the processor units (claims 1) or interface units (claim 7), and a second backplane to which plural disk units are connected. Additionally, under claim 13, it is possible to increase or decrease the number of processor units in a storage device in the case that an interface unit is not increased or decreased.

Further, under claim 17, the storage device includes an interface unit, a memory unit, and a processor unit, each mounted on a separate board connected to a first backplane, and a disk unit is mounted on a separate board connected to a second backplane. Thus, it is submitted that the present invention is patentable over the art of record because the art of record fails to disclose or suggest a storage device having a first backplane to which an interface unit, a memory unit, and a processor unit mounted on boards are connected, while a second backplane has a disk device connected thereto. Further, the present invention is patentable because the prior art does not show or suggest a first backplane having multiple

connectors for increasing or decreasing the number of processor units or interface units, while a second backplane has disk drives connected thereto.

B. Discussion of the References

None of the following references disclose a storage device having a first backplane with plural connectors for increasing or decreasing the number of processor units or interface units as set forth in independent claims 1, 7, and 13. Nor do they teach an interface unit, a memory unit, and a processor unit, each mounted on a separate board connectable to a backplane as set forth in independent claim 17.

1. U.S. Patent No. 6,820,171 B1

The patent to Weber, US 6820171, shows a method and structures for an extensible RAID storage architecture. In the system the front-end host interface control is separated from back-end disk array control and are interconnected using storage area networking (SAN) switching devices. Each FEC and BEC includes a SAN interface. Alternative embodiments include a SAN interface that is a pair of PCI bus interfaces each connected to one of two PCI bus backplanes. In this configuration, the SAN switch is simply the passive PCI backplane. The front-end control element for the storage subsystem comprises: a host system interface, a processor coupled to the host system interface to process host system generated I/O requests received through the host system interface; and a SAN interface coupled to the processor for coupling the front-end control element to a plurality of back-end control elements. See, e.g., Abstract; Figures 1-4; column 2, lines 40-67; column 3, lines 1-20, 35-67, and column 4. However, Weber does not teach the use of a first backplane with plural connectors for increasing or decreasing the number of processor units or interface units as set forth in claims 1, 7, and 13. Nor does Weber teach the use of separate boards connectable to a backplane as set forth in claim 17.

2. U.S. Patent Publication No. 2002/0188786 A1

The published U.S. patent application to Barrow, US 20020188786, shows a data storage system with integrated switching. A network adapter is provided that is used in a network data storage system to facilitate data communication among external data exchanging devices and an I/O controller residing in the system. The data storage system

includes a set of mass storage devices to exchange data with the data exchanging devices via the adapter. The adapter may include one or more interfaces that may be physically coupled to an electrical backplane in the system. The backplane is coupled to the controller, and may be configured to permit data communication between the controller and the adapter when the interfaces are coupled to the backplane. The adapter includes an integrated switching system that has a first set of ports that may be coupled to the data exchanging devices and a second set of ports that may couple the switching system to the controller when one or more interfaces are coupled to the backplane. See, e.g., Abstract; Figures 1-6; and paragraphs [0006]-[0013], [0027],[0034]-0040], and [0048]-[0050]. However, Barrow does not teach the use of a first backplane with plural connectors for increasing or decreasing the number of processor units or interface units as set forth in claims 1, 7, and 13. Nor does Barrow teach the use of separate boards connectable to a backplane as set forth in claim 17.

3. U.S. Patent Publication No. 2004/0098529 A1

The published U.S. patent application to Sangveraphunski, US 20040098529, shows an information handling system having integrated internal scalable storage system. The system includes a housing, a processor disposed in the housing, and a memory device for storing a program of instructions executable by the processor. A bus is also disposed in the housing, and the processor and the memory are coupled to the bus. A host bus adapter is also coupled to the bus, and an information storage system is coupled to the host bus adapter. The information storage system includes a backplane for coupling at least one information storage device to the host bus adapter. The information storage system and host bus adapter are compliant with a scalable, switching, mass storage system standard such as Fibre Channel. See, e.g., Abstract; Figures 1-4; and paragraphs [0004]-[0005], and [0013]-[0017]. Thus, while Sangveraphunski teaches a backplane 218 having storage devices coupled thereto, he does not teach does not teach the use of a first backplane with plural connectors for increasing or decreasing the number of processor units or interface units as set forth in claims 1, 7, and 13. Nor does Sangveraphunski teach the use of separate boards connectable to a backplane as set forth in claim 17.

4. U.S. Patent Publication No. 2004/0177182 A1

The published U.S. patent application to Metevier, US 20040177182, shows an embedded control and monitoring of hard disk drives in an information handling system. The information handling system has at least one SCSI disk drive, the system comprising: a motherboard; an embedded server management (ESM) interface attached to and in electrical communication with the motherboard; a RAID on motherboard (ROMB) controller attached to and in electrical communication with the motherboard; a SCSI accessed fault tolerant enclosure (SAF-TE) backplane having sensors, an input-output (I/O) interface and at least one SCSI connector; and at least one SCSI disk drive coupled to the at least one SCSI connector. See, e.g., Abstract; Figures 1-6; and paragraphs [0011]-[0017] and [0028]-[0032]. Thus, while Metevier also teaches a hard disk backplane having storage devices coupled thereto, Metevier does not teach does not teach the use of a first backplane with plural connectors for increasing or decreasing the number of processor units or interface units as set forth in claims 1, 7, and 13. Nor does Metevier teach the use of separate boards connectable to a backplane as set forth in claim 17.

5. U.S. Patent Publication No. 2004/0199719 A1

Of the art of record, the most relevant is believed to be the published U.S. patent application to Valin, US 20040199719, which shows a standalone network storage system enclosure including head and multiple disk drives. In one embodiment, the system includes a single-board storage server head 64 having a circuit board with a processor, a memory coupled to the processor, and a communication adapter coupled to the processor. A backplane 51 has a plurality of connectors for receiving single-board server heads 64 or I/O modules 31. One or more single-board server heads may be connected to backplane 51, which also has a plurality of disk drives connected thereto, for creating a stand-alone storage system. Alternatively, a single server head 1 may be included in a rack and connected to a plurality of external disk drive shelves 2. See, e.g., Abstract; Figures 1-9; and paragraphs [0024]-[0030] and [0038]-[0043]. Thus, Valin teaches the addition of multiple single-board server heads to the same backplane to which disk drives are connected, or the use of a single server head with one or more backplanes having disk drives connected. Accordingly, Valin does not teach a backplane to which processors or interfaces may be added or subtracted that is separate from a backplane having disk drives connected, as set forth in claims 1, 7, and 13. Nor does Valin teach an interface unit, a memory unit, and a processor unit, each mounted on

a separate board connected to a first backplane, as set forth in claim 17. Accordingly, claims 1, 7, 13, and 17 are believed to be patentable over Valin.

6. U.S. Patent Publication No. 2005/0010715 A1

The published U.S. patent application to Davies, US 20050010715, shows a network storage appliance with integrated server and redundant storage controllers. The appliance includes a chassis, a backplane enclosed in the chassis, and a server, enclosed in the chassis, coupled to the backplane. The appliance also includes a plurality of storage controllers enclosed in the chassis, each coupled to the backplane, and which control transfer of data between the server and a plurality of storage devices coupled to the plurality of storage controllers. The plurality of storage controllers also control transfer of data between the plurality of storage devices and a plurality of computers networked to the appliance and external to the appliance. The appliance includes first and second redundant active failover blades enclosed in a chassis, and hot-replaceable in a backplane of the chassis. Each of the first and second blades includes a processor that performs RAID functions to control storage of data on a plurality of storage devices, and a buffer memory, coupled to the processor, which buffers the data received from the plurality of storage devices. See, e.g., Abstract, figures 1-25, paragraphs [0011]-[0014], [0041]-[0050], [0057]-[0058], [0070]-[0075]. However, Davies does not teach the use of a first backplane with plural connectors for increasing or decreasing the number of processor units or interface units as set forth in claims 1, 7, and 13. Nor does Davies teach the use of separate boards connectable to a backplane as set forth in claim 17.

7. U.S. Patent No. 6,385,681

The patent to Fujimoto et al. (6,385,681) discloses a disk array control device which includes a plurality of channel interface (IF) units, a plurality of disk IF units, a cache memory unit, and a shared memory unit. The connection system between the plurality of channel IF units and plurality of disk IF units and the cache memory unit is different from the connection system between the plurality of channel IF units and plurality of disk IF units and the shared memory unit. The plurality of channel IF units an the plurality of disk IF units are connected via a selector to the cache memory unit, whereas the plurality of channel IF units

and the plurality of disk IF units are directly connected to the shared memory unit with no selectors.

As discussed in the present application at pages 3-4, all the channel IF units 11 and all the disk IF units 16 control data transfer between the channel IF unit 11 and the disk IF unit 16 via the cache memory unit 14 and the control information memory unit 15. Therefore, if the data transfer processing performance of the channel IF unit 11 an the disk IF unit 16 improves, the access load to the cache memory unit 14 and the control information memory unit increases. This results in an access load bottleneck, which makes it difficult to improve performance of the storage system 8 in the future. In other words, the scalability of performance cannot be guaranteed. If the scale of the cache memory unit 14 and the control information memory unit 15 is increased, decreasing the cost of the storage system in a small scale configuration is difficult, and providing a storage system with a small scale configuration at low cost becomes difficult.

The reference does not disclose a storage device having a first backplane with plural connectors for increasing or decreasing the number of processor units or interface units, as recited in claims 1, 7, and 13; or an interface unit, a memory unit, and a processor unit, each mounted on a separate board connectable to a backplane, as recited in claim 17.

8. U.S. Patent No. 6,542,961

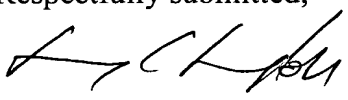
The patent to Matsunami et al. (6,542,961) discloses a disk storage system containing a storage device having a record medium for holding the data, a plurality of storage sub-systems having a controller for controlling the storage device, a first interface node coupled to a computer using the data stored in the plurality of storage sub-systems, a plurality of second interface nodes connected to any or one of the storage sub-systems, a switching means connecting to a first interface node and a plurality of second interface nodes to perform frame transfer between a first interface node and a plurality of second interface nodes based on node address information added to the frame. The first interface node has a configuration table to store structural information for the memory storage system and in response to the frame sent from the computer, analyzes the applicable frame, converts information relating to the transfer destination of that frame based on structural information held in the configuration table, and transfers that frame to the switching means.

As discussed in the present application at pages 3-4, the scalability of performance is present. However, the server 3 accesses the disk array system 4 via the disk-array-switches 5. Therefore, in the interface unit with the server 3 of the disk-array-switch 5, the protocol between the server and the disk-array-switch is transformed to a protocol in the disk-array-switch, and in the interface unit with the disk array system 4 of the disk-array-switch 5, the protocol in the disk-array-switch is transformed to a protocol between the disk-array-switch and the disk array systems, that is, a double protocol transformation process is generated. Therefore, the response performance is poor compared with the case of accessing the disk array system directly, without going through the disk-array-switch.

The reference does not disclose a storage device having a first backplane with plural connectors for increasing or decreasing the number of processor units or interface units, as recited in claims 1, 7, and 13; or an interface unit, a memory unit, and a processor unit, each mounted on a separate board connectable to a backplane, as recited in claim 17.

(f) In view of this petition, the Examiner is respectfully requested to issue a first Office Action at an early date.

Respectfully submitted,



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60459826 v1